HERMETIC CHIP-SCALE PACKAGE FOR PHOTONIC DEVICES

BACKGROUND

The Government may have rights in this invention pursuant to Contract No. F30602-97-2-0120, awarded by the Department of the Air Force.

Optical coupling and electrical connections to photonic devices, particularly arrays of them on a single chip, are subject to environmental effects, electrical parasitics, and mechanical misalignment. There appears to be no adequate packaging approaches available to effectively eliminate these problems and at the same time provide ruggedized, compact, high-performing and reliable systems.

SUMMARY OF THE INVENTION

The invention is a hermetic packaging of optical emitters and/or detectors via bump bonding on an electrically patterned transparent window. It is to simultaneously provide sealed containment or hermeticity and optical coupling to VCSEL's or detectors, either in arrays or as single devices. These devices or device are

made of a semiconductor such as gallium arsenide. Hermeticity is often required for environmentally sensitive devices. No such hermetic array package is known.

The semiconductor is bump bonded to a window patterned with electrically conductive traces, which is itself sealed at the periphery to a ceramic or similar package. Electrical connections to, say, multi-layer impedance controlled traces external to the sealed cavity are accomplished within the ceramic package. The window may be equipped with refractive or diffractive lenses to improve optical coupling into and out-of the package. The optical devices and corresponding lenses may be in the form of one or two-dimensional arrays. Fibers being optically connected to an array of devices may be in the form of a ribbon or cord having a multitude of fibers for conveying light to or from the devices. Mechanical features are included to provide passive or semi-active alignment to a second level package that encompasses the first level package containing the optical devices. The package may be used in conjunction with an optical back plane. This approach provides precision optical coupling alignment, mechanical ruggedness, compactness, optical and electrical isolation, very low parasitics, high speed performance, protection from moisture, humidity and other dehabilitating

contaminants of the ambient environment, device reliability, and fabrication advantages.

BRIEF DESCRIPTION OF THE DRAWING

Figure 1a shows a hermetic 1st-level package for optical devices and their optical and electrical couplings, both to board-level electrical pads and to optical fibers via the indicated 2nd-level package assembly.

Figure 1b provides a view of the optical coupling between optical fibers and a photonic device.

Figure 2a shows a window having metal traces and mechanical registration features formed on it.

Figure 2b reveals a housing having photonic devices, the electrical interconnects of which match up with the corresponding interconnects on the window.

Figures 3a and 3b illustrate a housing having a pin arrangement for connecting and securing a ferrule or plug having the optical light wave guides or fibers that are brought next to the window.

Figures 4a and 4b shows a perspective view of a plug and housing having the pin arrangement.

DESCRIPTION OF THE EMBODIMENTS

Figure 1a shows a hermetic chip scale package 10 for photonic devices. To attain hermeticity and efficient optical coupling to a linear or 2-dimensional array of VCSEL's 11 and/or detectors 12, the semiconductor die containing the VCSEL's or detectors is bump bonded to a partially metalized window 13 at electrically conductive bump 14. Window metallization 28 can be some combination Cr, Pt, Au, Ti, Cu, ITO, or Ni, either sputtered, evaporated, or plated. Window 13 is also sealed at the periphery to multi-layer ceramic package 15 with hermetic solder seal 16, while simultaneously completing chip-to-window electrical connection at conductive bump 14. Chip 11, 12 is attached to ceramic package 15 via electrical and/or thermal connection 17. Chip 11, 12 is hermetically sealed from an ambient environment 18 of device 10. Electrical connection 17 is connected to chip 11, 12 and to external pad 19 via conductive path 31. The pad at bump 14 is also connected to electrical path 31 via conductive trace 28 from chip 11, 12 to pad 51, and thereby to external electrical connection pad 20 via path 31. A refractive and/or diffractive optical element 58 may be etched into or deposited on a surface of the window to

facilitate improved optical coupling efficiency. The package, so far described, is a first level package.

A second level package is housing 21 and fits on and around the first level package encompassing chip 11, 12 within a hermetic seal. Housing 21 is mechanically aligned with one or more keys 22 on window 13. Ferrule 23 is inserted within housing 21 and may be slid into a position where an edge 24 of the ferrule buts up against key or keys 22. Situated in ferrule 23 is a fiber or fibers 25, which convey light signals 26 from VCSEL's 11, and/or light signals 27 to detectors 12. Housing 21 may be secured to the first level housing with glue, adhesive or an epoxy. Once ferrule 23 is inserted all the way into housing 21, it may or may not be glued into place.

Figure 1b shows a closer view of the optical coupling between fiber 25 and photonic device 11, 12. Light comes or goes through core 53 of fiber 25. Cladding 54 covers and protects glass core 53. Cladding has an index of refraction so as to contain the light within core 53. Fiber 25 butts up against window 13. Window 13 has a thickness 55 that ranges from roughly 25 to 250 microns. The index of refraction of the material of window 13 is about 1.52. That index may vary dependent on the particular design of package 10. Between window 13 and the

emanating or sensing portion 57 of device 11, 12, there is a gap 56 of about 25 microns.

Figure 2a shows window 13 onto which first level housing 15 is adhered via solder seals 16. Light signal source 11 or detector 12 is bump bonded to transparent window 13 via electrically conductive or metal traces 28 on the surface of window 13 and metal terminals 29 on chip 11, 12 with solder bumps 14. Metalization strips 28 may have lateral dimensions of 20 to 50 microns, and thicknesses of less than 5 microns. Chip 11, 12 is typically between 3 and 8 millimeters. Window 13 may be composed of a material such as quartz or sapphire. Solder ring 16 may be composed of tin in combination with lead, gold or silver. Solder bumps 14 may be composed of tin in combination with lead, gold or silver.

Figure 2b illustrates housing 15 having optical devices 11, 12 with electrical connecting spots 58 that match up with conductive strips 28 so as to electrically connect sensitive areas 57 of devices 11, 12 with connecting spots 29. External connections 20 are connected in housing 15 to connecting spots 29.

Figure 3a shows an embodiment 40, which utilizes a pin 42 to hold plug or ferrule 43 to housing 41. Figure 3a shows a cut-away section along pin 42. Figure 3b, on the

other hand, shows a cut-away section along fiber 25 and emanation or receptor area 57. Ferrule 43 has an edge 44 which is butted up against bumper 45, which may be an elastomeric seal, as shown in figure 3b. Pin 42 is inserted through an alignment hole 51 in ferrule 43 and alignment hole 52 in housing 41 and is secured in place with a retaining clip 46 inserted in notch 47 at the end of pin 42. Ferrule 43 is held firmly in place with the tension of a loading spring 48 between ferrule 43 and clip or shoulder 49 at the end of pin 42, which is opposite of the end having notch 47. Pin 42 and holes 51 and 52 provide a less than the plus or minus five micron alignment between fiber 25 and VCSEL 11 or detector 12 emanation or receptor area 57, respectively, as shown in figure 3b. Since ferrule 43 is not glued to housing 41, it may be removed whenever desired by removing clip 46 from notch 47. Chip 11, 12 according to embodiment 40 is hermetically sealed. However, one may choose to have chip 11, 12 not hermetically sealed by replacing the multi-layer ceramic package with an FR4 or equivalent plastic package in cost-reduced embodiment 40.

An arrangement, as shown in figures 4a and 4b, has one or more pins 42 holding a ferrule 43 with a fiber array 25 to housing 41. Pins 42 and respective holes 51 and 52 are

placed on each side of fiber array 25 for secure, robust and precision alignment of fiber array 25 with lens 37 and sensitive or emanating area 57 of chip 11, 12.

In another embodiment, plug or ferrule 43 may be part of a backplane, and housing 41 may be attached to an opto-component circuit board, which is plugged into the backplane via plug 43 and housing 41.

Other embodiments and variants of the present invention, not disclosed here, are covered by the claims and only limited in scope by the claims, which includes all equivalents thereof.